REMARKS

Claims 1-23 are pending. Claims 1-23 are rejected. Applicants respectfully request reconsideration of the present application in view of the amendments above and the remarks set forth below.

INFORMATION DISCLOSURE STATEMENT

The Office Action recites that the Information Disclosure Statement of 10/18/04 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. However, submission of these copies is not required under 37 C.F.R. § 1.98(d)(1) because the present application claims priority to U.S. patent application number 10/630,542 under 35 U.S.C. § 120 in which the copies of the references have already been submitted.

Applicants have submitted an Information Disclosure Statement for the Heybruck reference for consideration.

DRAWINGS OBJECTIONS UNDER 37 C.F.R. 1.84(m)

Applicants have resubmitted FIGS. 9 and 10 to clarify the legibility of the elements contained therein. Applicants do not enter any new matter by resubmitting FIGS. 9 and 10.

DRAWINGS OBJECTIONS UNDER 37 C.F.R. 1.83(a)

FIG. 9 depicts the memory 910 and incrementing the memory address (e.g. 0x100) through the instructions 905, 915, 925, 935, and 945 to support claim 6. Furthermore, FIG. 10 depicts the memory 1030 for PUT instructions in the incrementing direction to support claim 13.

The decrementing through memory is supported by the WRGETINIT(D,A) instruction by specifying decrement or increment disclosed in paragraph 65 in the Specification and shown in code in paragraph 73 in the Specification. Thus, the drawings objections under C.F.R. 1.83(a) are overcome by FIGS. 9 and 10 and the Specification.

CLAIM OBJECTIONS

Claims 13, 19, 20, and 23 are objected for informalities.

Claim 13 is objected for "the next aligned word." Applicants have amended claim 13 to recite "a next aligned word."

Claims 19, 20, and 23 are objected for the phrase "stored as an index in a register memory." Applicants note that the "specified number" can be stored "as" an index in a register memory and not stored at "an index." Paragraph 81 discloses a GET instruction that retrieves a number of bits that is specified in a register (e.g. address register).

REJECTIONS UNDER 35 U.S.C. § 101

Claims 17-23 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The Office Action recites that "[c]laims 17-23 are not limited to tangible embodiments". Applicants have amended claims 17-23 to recite a system that comprises a load/store buffer and a processor that executes instructions. (Supported in FIG. 8) Because the system has tangible embodiments, the rejections under 35 U.S.C. 101 are moot.

REJECTIONS UNDER 35 U.S.C. § 112

Claims 17-23 are rejected under 35 U.S.C. 112, second paragraph for being indefinite. Applicants have amended claims 17-23 to recite multiple GET or PUT instructions to further clarify the invention. Thus, the rejections under 35 U.S.C. 112 should be removed.

REJECTIONS UNDER 35 U.S.C. § 102(b)

Claims 1-3, 5-6, 8-10, 12-13, and 15-23 are rejected under 35 U.S.C. 102(b) as being unpatentable over U.S. Patent No. 5,517,627 to Petersen (hereinafter "Petersen"). Further, U.S. Patent 5,636,224 to Voith et. al. (hereinafter "Voith") is used to support an inherent feature of Petersen.

Amended claim 1 recites the steps of initializing a load/store buffer by loading a first aligned word of fixed length into the load/store buffer from memory and reading one or more data sequences from the load/store buffer into a register file for instruction execution. (Supported in paragraph 64 of the Specification)

Petersen discloses a data aligner including a write data aligner and a read data aligner for alignment of data segments (Abstract and Field of the Invention). The alignment of data segments in Petersen occurs in a peripheral device, such as a network adapter (col. 1, line 26). As depicted in FIG. 8 and described in the Field of the Invention, the alignment of data segments is in the context of transferring data between a host bus and a buffer. The buffer memory in FIG. 8 of Petersen is a FIFO buffer. However, the context in which amended claim 1 occurs is different from the context in which Petersen occurs. Amended claim 1 recites the loading of an aligned word is from memory into a load/store buffer and the reading of the data sequences is from the

load/store buffer into a register file for instruction execution. Amended claim 1 occurs in the context of loading and storing data between memory and a register file for instruction execution using a load/store buffer as opposed to transferring data between a bus and a buffer memory for a peripheral device as in Petersen.

Furthermore, Petersen does not teach or suggest a register file for instruction execution as recited in amended claim 1. Petersen does teach queuing registers in col. 8, lines 29-47 and FIGS. 5A-B. However, the registers taught in Petersen are queuing registers to "preserve the previous read value from the buffer" (col. 8, lines 30-33). The queuing registers in Petersen are not a register file for instruction execution. Register files that stores values that a processor uses when executing an instruction differ from a queuing register that merely stores previous read values. Therefore, Petersen does not anticipate the register file for instruction execution as recited in claim 1. Thus, claim 1 is allowable for at least the above stated reasons over Petersen.

Claims 15 and 17 have been amended to include similar limitations as amended claim 1 and are allowable for at least the same reasons as claim 1 over Petersen.

In regards to claims 8, 16, and 21, the Office Action recites that the "rejection follows similarly to the rejection of claims 1, 15, and 17." Amended claim 8 recites initializing a load/store buffer by filling the load/store buffer with one or more unaligned data sequences from a register file for instruction execution. As discussed above, Petersen does not teach or suggest a register file for instruction execution. Thus, Petersen does not teach the limitation of initializing a load/store buffer by filling the load/store buffer with one or more unaligned data sequences from a register file for instruction execution as recited in amended claim 8. Thus, claim 8 is allowable for at least the above stated reasons over Petersen.

Claims 16 and 21 have been amended to include similar limitations as amended claim 8 and are allowable for at least the same reasons as claim 8 over Petersen.

Claims 2 and 3 are dependent on claim 1 and are allowable for at least the same reasons as claim 1 over Petersen.

Claims 5 and 12 are dependent on claims 1 and 8 respectively and are allowable for at least the same reasons as claim 1 over Petersen. Additionally, claim 1 recites a method for processing data sequences of arbitrary length in a computing system. Claim 5 recites wherein the computing system comprises a general-purpose processor. The Office Action recites the host processor 10 in FIG. 7 of Petersen to teach the general-purpose processor of claim 5. However, the processing of data sequences of arbitrary length occurs in the data aligner (Abstract and Summary of the Invention), which as depicted in FIG. 7 is in the peripheral device 15 that is separate from the host processor 10. The processing of data sequences in Petersen does not occur in the computing system, which can be a general-purpose processor, as recited in claims 1 and 5. Thus, claims 5 and 12 are allowable for at least the above stated reasons over Petersen.

Claims 6 and 13 are dependent on claims 1 and 8 respectively and are allowable for at least the same reasons as claims 1 and 8 over Petersen.

Claims 9 and 10 are dependent on claim 8 and are allowable for at least the same reasons as claim 8 over Petersen.

Claims 18-20 are dependent on claim 17 and are allowable for at least the same reasons as claim 17 over Petersen.

Claims 22-23 are dependent on claim 21 and are allowable for at least the same reasons as claim 21 over Petersen.

REJECTIONS UNDER 35 U.S.C. § 103

Claims 4 and 11 are rejected under 35 U.S.C. 103 as being unpatentable over Petersen in view of U.S. Patent 5,619,665 to Emma (hereinafter "Emma").

Claims 4 and 11 are dependent on claims 1 and 8 respectively and are allowable for at least the same reasons as claims 1 and 8 over Petersen. Additionally, in regards to claims 4 and 11, the Office Action recites that Petersen "does not specifically teach a processor having an extensible instruction set." Emma teaches a translation engine for translating sequences of old architecture instructions into primary, new architecture instructions into primary, new architecture instructions (Abstract). Emma also teaches an extended instruction cache memory for storing the translations. The Office Action recites that "it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the data aligner system of figure 7 with the teaching of an extension instruction set of Emma in order to have gained expandability of the instruction set of the processor 10 of Petersen, thereby gaining flexibility and compatibility for future instruction extensions without having to recompile or reassemble the system of Petersen." Applicants respectfully traverse this motivation to combine Petersen and Emma.

The concept of the data alignment in a data aligner in a peripheral device of Petersen is unrelated to the concept of translations for extended instructions using the translation engine and extended instruction cache memory of Emma. The data aligner in Petersen does not perform instruction processing so there is no need to extend the instruction set as taught in Emma. While Petersen does teach a processor 10 in FIG. 7, Petersen does not mention instruction execution for the processor 10, and the data alignment in Petersen all occurs in the peripheral device 15. Because the operations of the peripheral device for data alignment in Petersen is unrelated to the

extended instruction processing in Emma, thus, one skilled in the art would not have combined Petersen with Emma. Thus, claims 4 and 11 are allowable for at least the above stated reasons over Petersen and Emma.

REJECTIONS UNDER 35 U.S.C. § 103

Claims 7 and 14 are rejected under 35 U.S.C. 103 as being unpatentable over Petersen in view of U.S. Patent 5,636, 224 to Voith et. al. (hereinafter "Voith").

Claims 7 and 14 are dependent on claims 1 and 8 respectively and are allowable for at least the same reasons as claim 1 and 8 over Petersen.

CONCLUSION

Therefore, in view of the above remarks this application is in condition for allowance, and the Examiner is respectfully requested to allow this application. The Examiner is invited to contact Applicants' undersigned representative regarding any issues that the Examiner feels are still outstanding.

Respectfully submitted,

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